

B450 AORUS ELITE V2

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[illegible]

Model Name:B450 AORUS ELITE V2

Component value change history

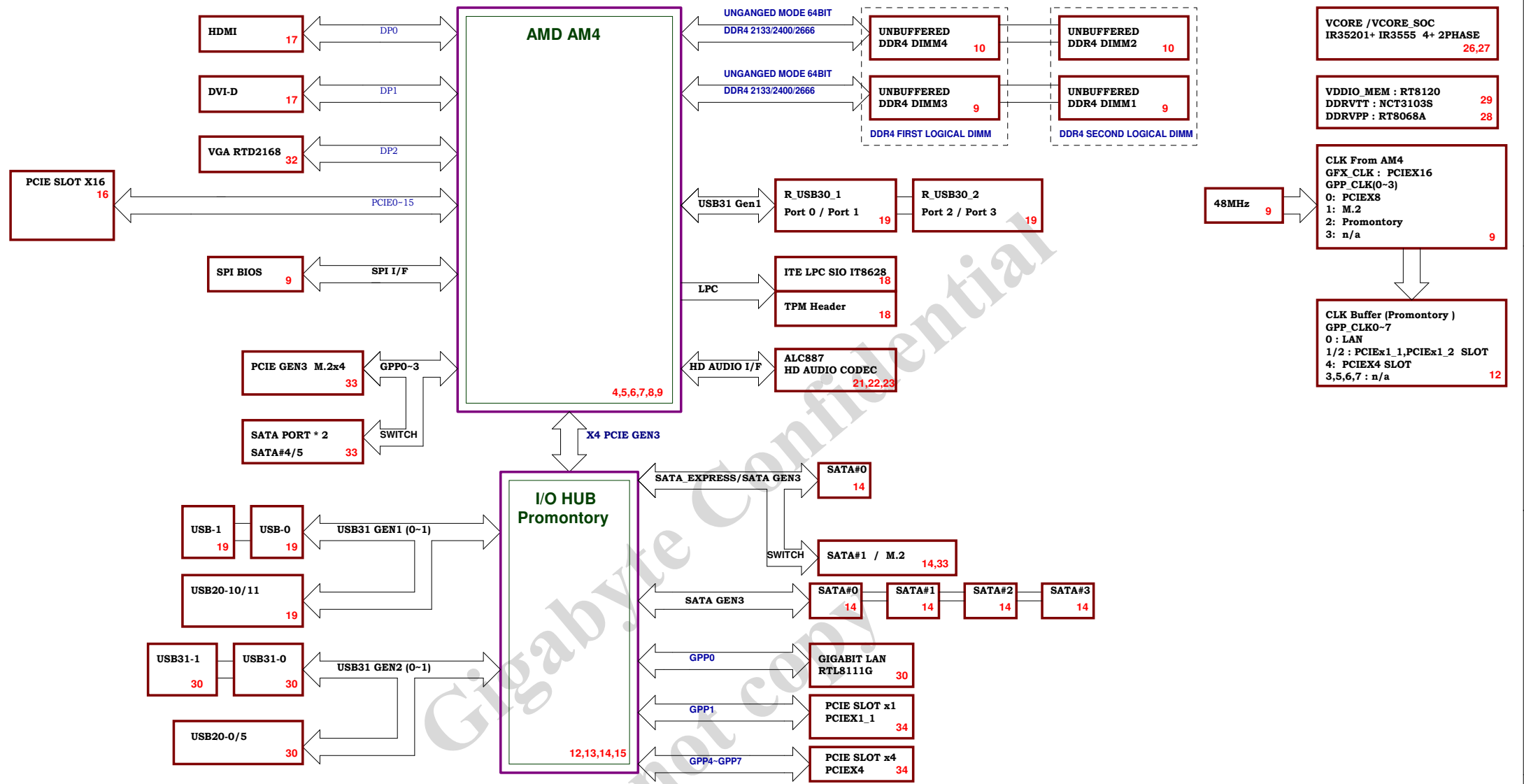
Version: 1.01

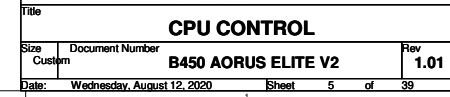
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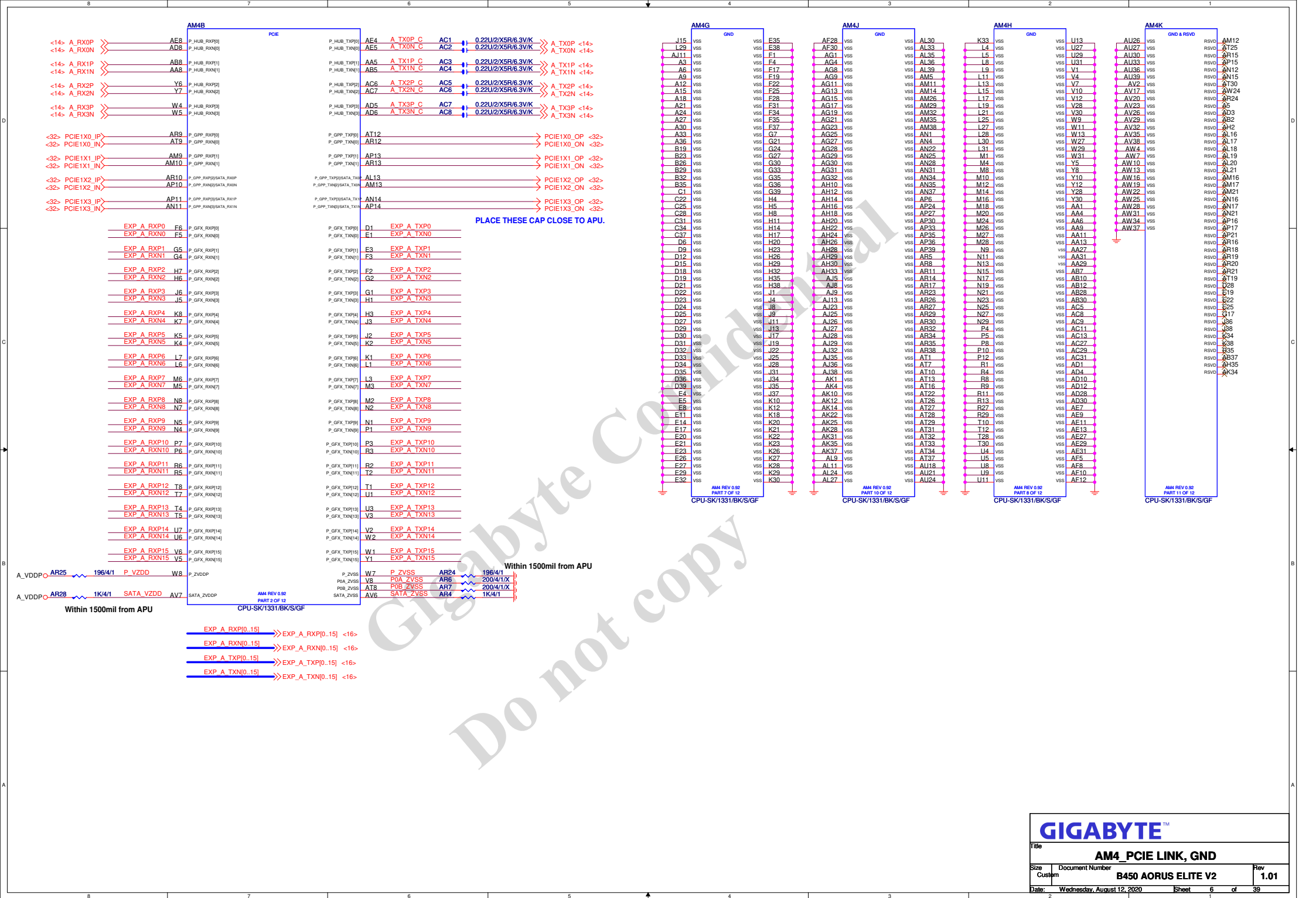
Date	Change Item		Reason
2017.02.23	10D P-BOM Release.	PCB: 1.0	1. AUDIO : 11CE2-651000-21R 2. NPEC1,EC31,EC24 : 11CO5-691000-11R /12R 3. 270U : 11CO5-8C2700-11R/12R 4. 560U : 11CO2-695600-21R/22R 5. HDMI : AZ1045-04F/MSOP10
2017.03.10			1. UPDATE EC FW TO V620.BIN
2017.04.27			1. UPDATE EC FW TO V622.BIN
2018.06.25	02 D-BOM Release.	PCB: 0.2	1. -MPD1 (LOCATION : FPESD) 2. LOCATION : PU6 pin30 原PE1_PSRNT- change to PE3_PSRNT- 3. location : M2BC17/M2BC13/M2BC18/M2BC19 請靠近m2b_socket 4. down size 0603 5. 新增旋甲 6. modify from B450 AORUS to B450 AORUS ELITE
2018.07.12	10 P-BOM Release.	PCB: 1.0	1. ECR50 for FAN 0 RPM PULL UP 2. MAR6/AR52/AR47/PR8 change to short-pad 3. KB_MS_USB 用料限制用-14R用料
2018.07.12	10B F-BOM Release.	PCB: 1.0	1. 修改ATX connect 用料:91高溫料 [11NH4-020024-Z1R_11NH4-020024-Z2R]
2018.08.20	10G D-BOM Release.	PCB:1.01	1. Vcore SENSE 位置 2. C125 10u change to 22u 3. VINA0 change to APU_PWRGD(for summit / Pinnacle 不上DIMM時,僅亮CPU DEBUD LED,應改為亮DDR DEBUD LED) 4. BRN1 change to 1K
2018.09.21	10G SKIP PVTRelease.	PCB:1.01	SKIP PVT
2019.05.21	10H SKIP PVTRelease.	PCB:1.01	1. UPDATE NEW EC FW V684.BIN
2019.07.08	10H ECN	PCB:1.01	1. Location :AIO_SHIELD 11AIO-0C0013-02R 加替料11AIO-0C0013-12R
2019.11.12	10M ECN	PCB:1.05	1. Vcore choke Footprint 自動插件修改
2020.06.22	10L ECN	PCB:1.05	1. 新增替代料 - IT8795 (10HP2-118795-10R) , 統一使用 IT8795 以利後續備料
2020.06.22	10P MP	PCB:1.05	1. SIO CX-->DX(10HP2-118686-40R) 2. BOM : 9MB45ARSE-00-10P(與10L並存)
2020.07.23	10A EVT	PCB:1.0	1. CHANGE PWM 2. SOC CHOKE CHANGR 11LC5-M5300C-01C 3. BOM : 9MB45AET2-00-10A
2020.08.04	10B PVT	PCB:1.01	1. DR19-->3.83K , DR46/DR47-->3.09K , DR16-->3.32K , DR44/DR45--> 2. Location: DU1 -->10TA1-63567B-07R 3. 3. BOM : 9MB45AET2-00-10B
2020.08.04	10B ECN	PCB:1.01	1. Location:DEL1,DFL1 新增 11LC5-F5300C-08R自動插件料號

Circuit or PCB layout change for next version

[illegible]

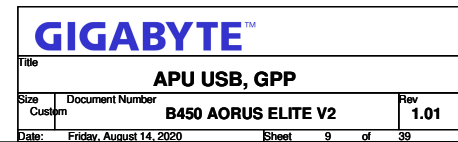
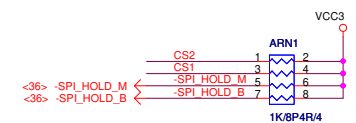


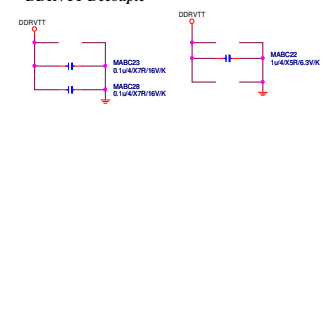
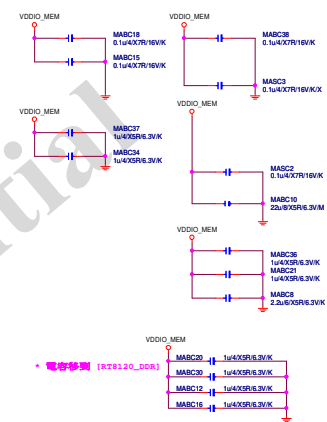
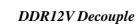
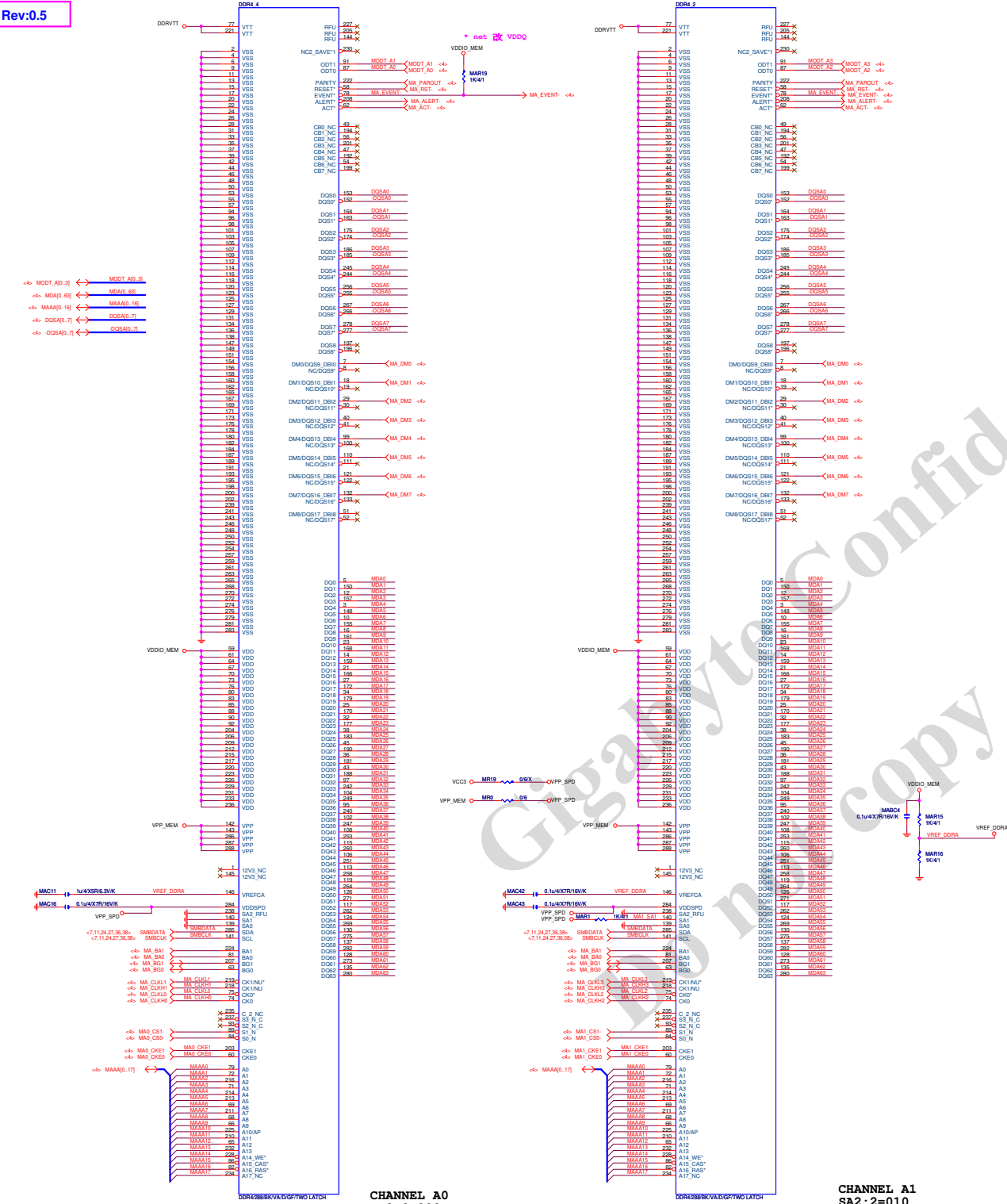


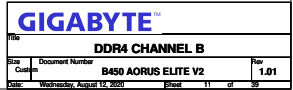


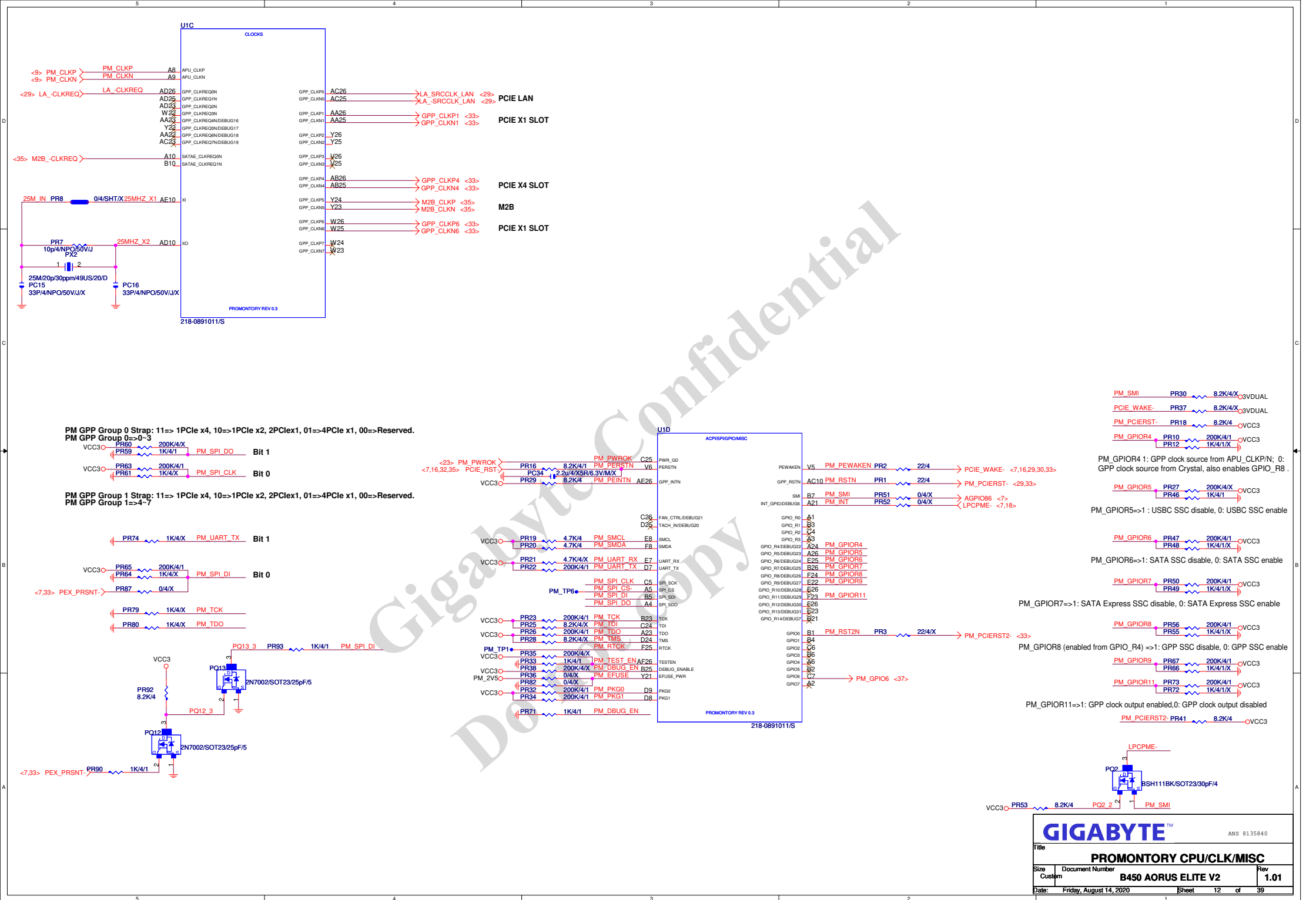
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SHORT	CLEAR CMOS
OPEN	NORMAL

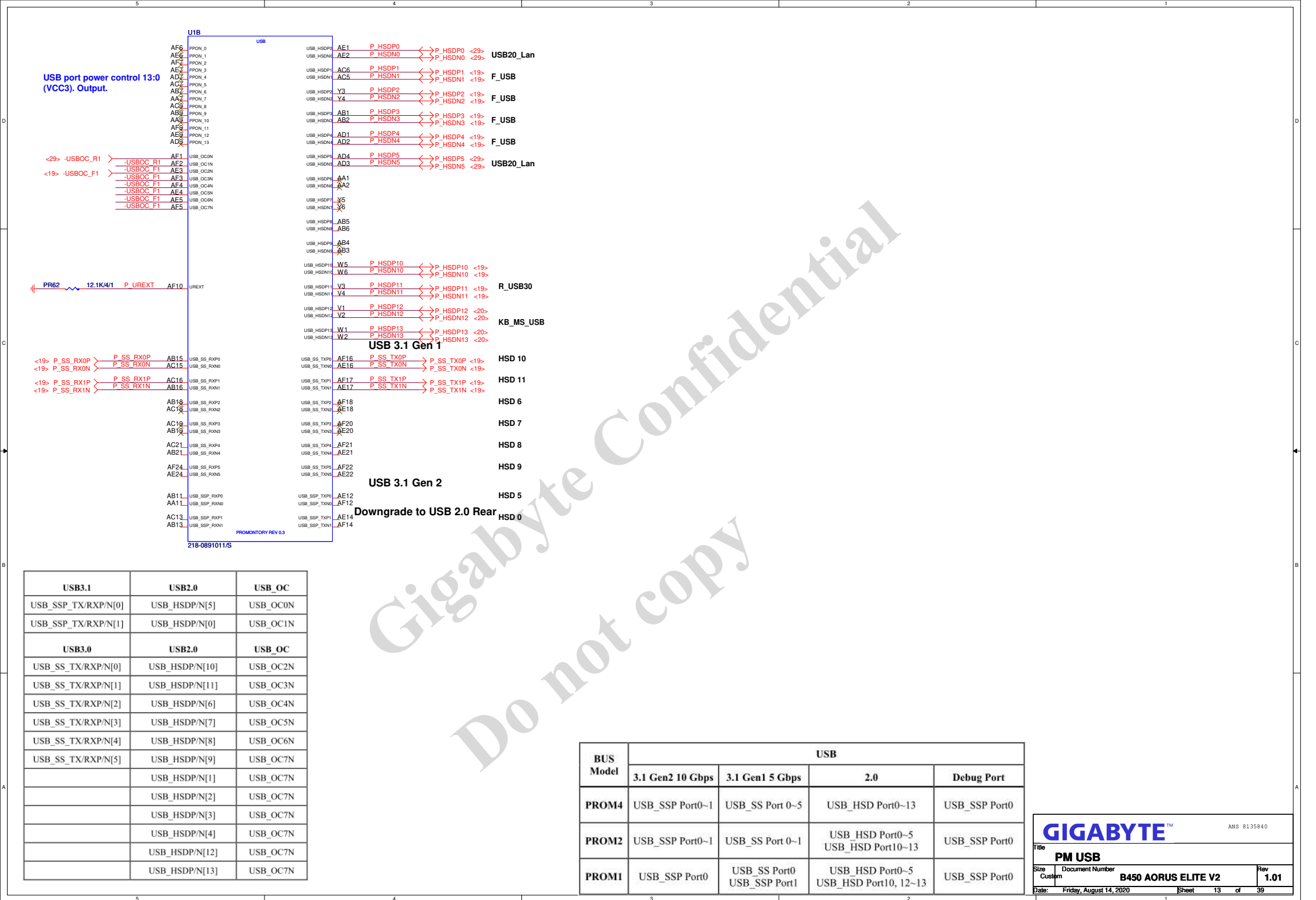
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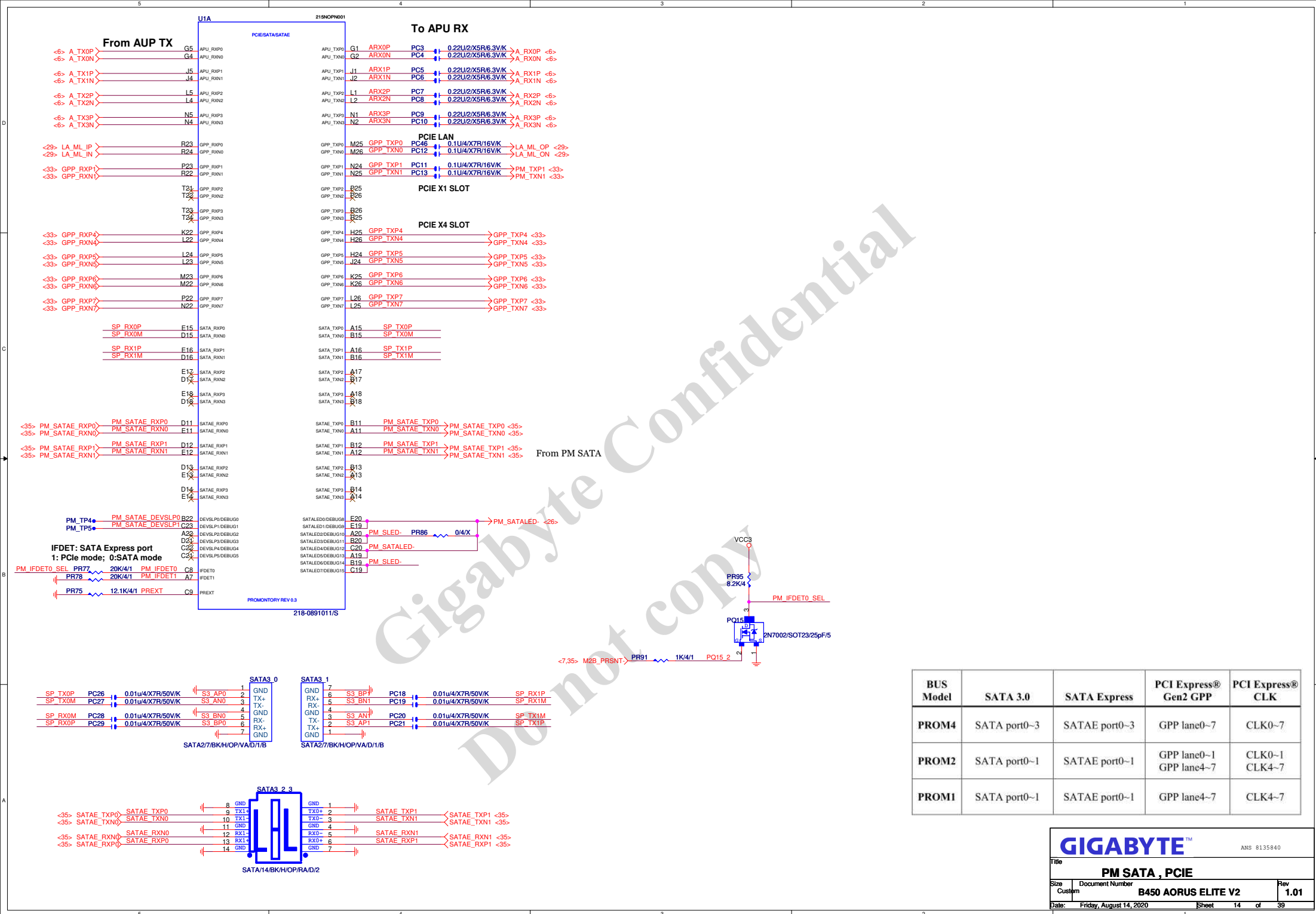




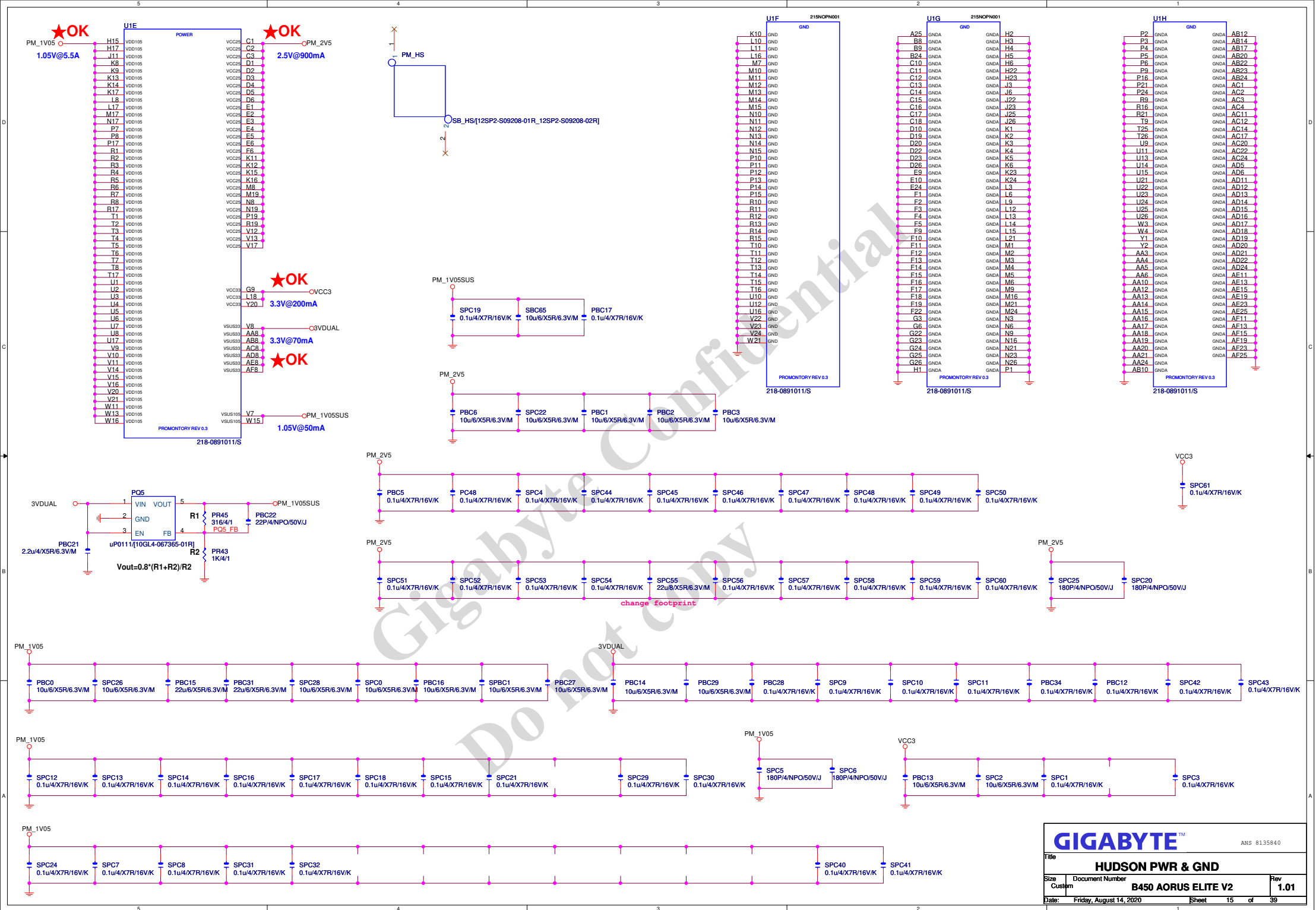


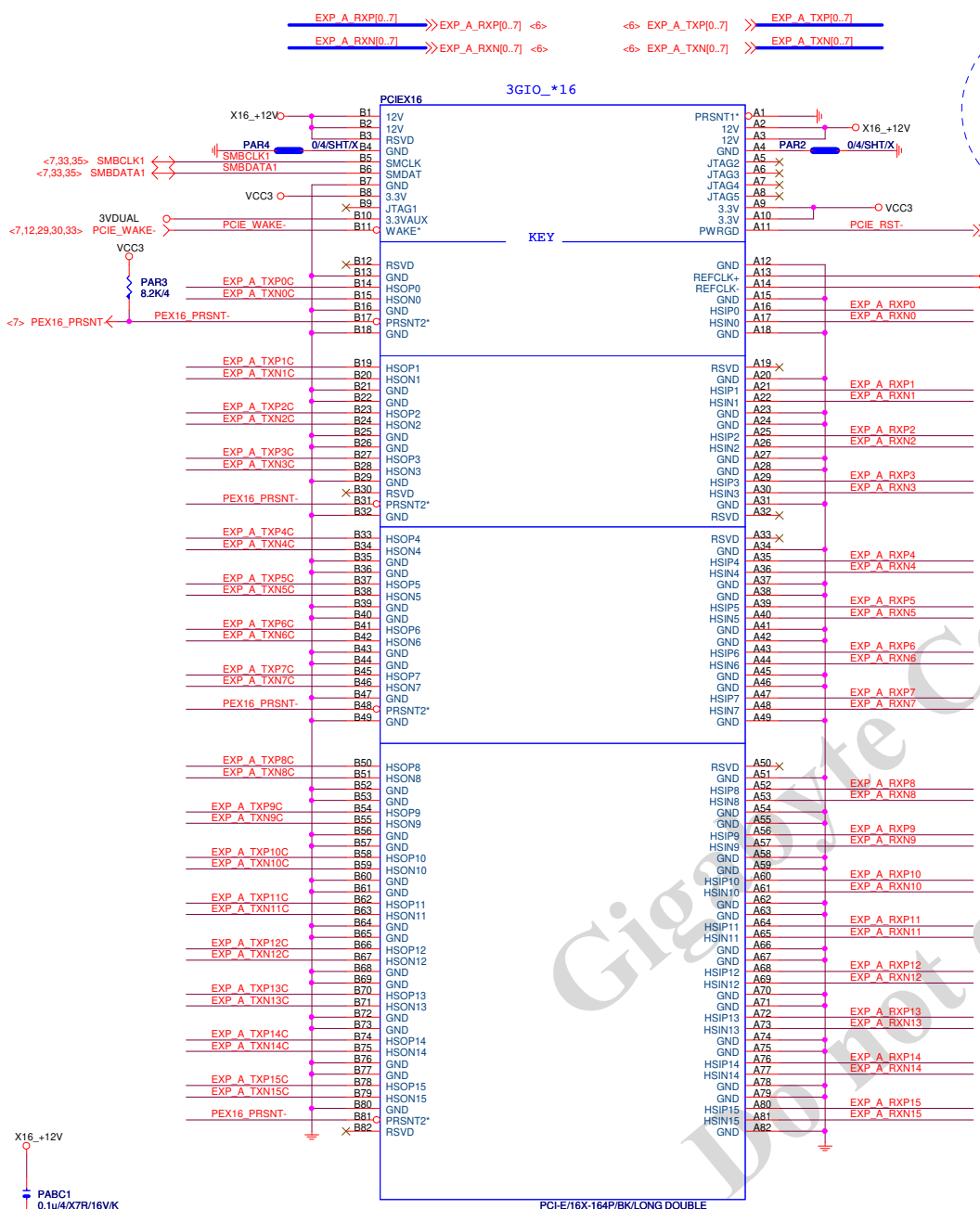






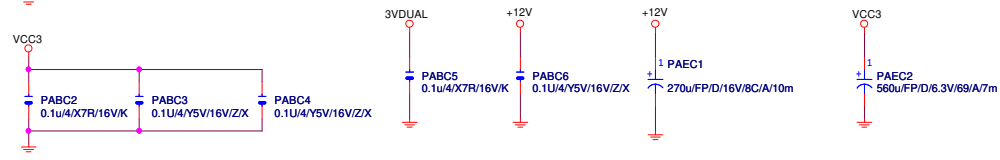
BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7





EXP A TXP0	PAC4	0.22U/2/X5R6.3V/K	EXP A TXP0C
EXP A TXN0	PAC5	0.22U/2/X5R6.3V/K	EXP A TXN0C
EXP A TXP1	PAC6	0.22U/2/X5R6.3V/K	EXP A TXP1C
EXP A TXN1	PAC7	0.22U/2/X5R6.3V/K	EXP A TXN1C
EXP A TXP2	PAC8	0.22U/2/X5R6.3V/K	EXP A TXP2C
EXP A TXN2	PAC9	0.22U/2/X5R6.3V/K	EXP A TXN2C
EXP A TXP3	PAC10	0.22U/2/X5R6.3V/K	EXP A TXP3C
EXP A TXN3	PAC11	0.22U/2/X5R6.3V/K	EXP A TXN3C
EXP A TXP4	PAC12	0.22U/2/X5R6.3V/K	EXP A TXP4C
EXP A TXN4	PAC13	0.22U/2/X5R6.3V/K	EXP A TXN4C
EXP A TXP5	PAC14	0.22U/2/X5R6.3V/K	EXP A TXP5C
EXP A TXN5	PAC15	0.22U/2/X5R6.3V/K	EXP A TXN5C
EXP A TXP6	PAC16	0.22U/2/X5R6.3V/K	EXP A TXP6C
EXP A TXN6	PAC17	0.22U/2/X5R6.3V/K	EXP A TXN6C
EXP A TXP7	PAC18	0.22U/2/X5R6.3V/K	EXP A TXP7C
EXP A TXN7	PAC19	0.22U/2/X5R6.3V/K	EXP A TXN7C
EXP A TXP8	PAC20	0.22U/2/X5R6.3V/K	EXP A TXP8C
EXP A TXN8	PAC21	0.22U/2/X5R6.3V/K	EXP A TXN8C
EXP A TXP9	PAC22	0.22U/2/X5R6.3V/K	EXP A TXP9C
EXP A TXN9	PAC23	0.22U/2/X5R6.3V/K	EXP A TXN9C
EXP A TXP10	PAC24	0.22U/2/X5R6.3V/K	EXP A TXP10C
EXP A TXN10	PAC25	0.22U/2/X5R6.3V/K	EXP A TXN10C
EXP A TXP11	PAC26	0.22U/2/X5R6.3V/K	EXP A TXP11C
EXP A TXN11	PAC27	0.22U/2/X5R6.3V/K	EXP A TXN11C
EXP A TXP12	PAC28	0.22U/2/X5R6.3V/K	EXP A TXP12C
EXP A TXN12	PAC29	0.22U/2/X5R6.3V/K	EXP A TXN12C
EXP A TXP13	PAC30	0.22U/2/X5R6.3V/K	EXP A TXP13C
EXP A TXN13	PAC31	0.22U/2/X5R6.3V/K	EXP A TXN13C
EXP A TXP14	PAC32	0.22U/2/X5R6.3V/K	EXP A TXP14C
EXP A TXN14	PAC33	0.22U/2/X5R6.3V/K	EXP A TXN14C
EXP A TXP15	PAC34	0.22U/2/X5R6.3V/K	EXP A TXP15C
EXP A TXN15	PAC35	0.22U/2/X5R6.3V/K	EXP A TXN15C

EXP A RXP[0..15] >>> EXP_A_RXP[0..15] <-6>
EXP A RXN[0..15] >>> EXP_A_RXN[0..15] <-6>
EXP A TXP[0..15] >>> EXP_A_TXP[0..15] <-6>
EXP A TXN[0..15] >>> EXP_A_TXN[0..15] <-6>



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Size Custom

Date: Wednesday, August 12, 2020

Document Number

B450 AORUS ELITE V2

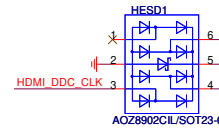
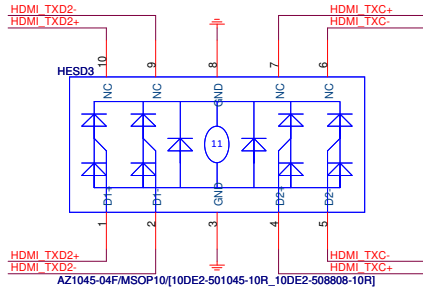
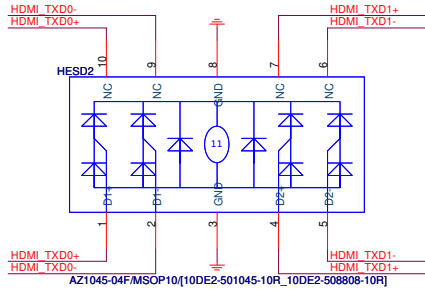
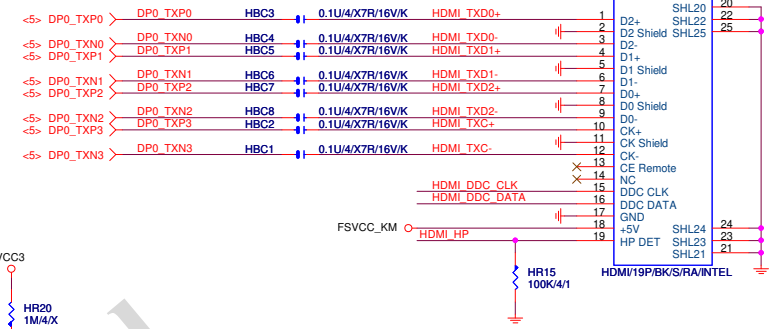
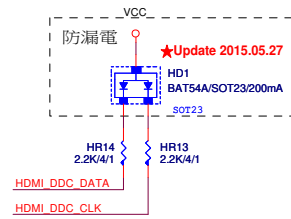
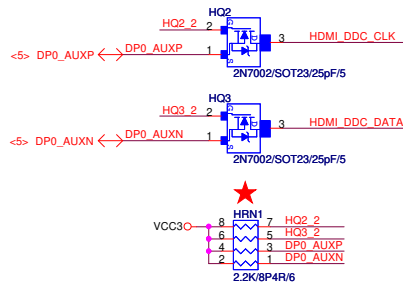
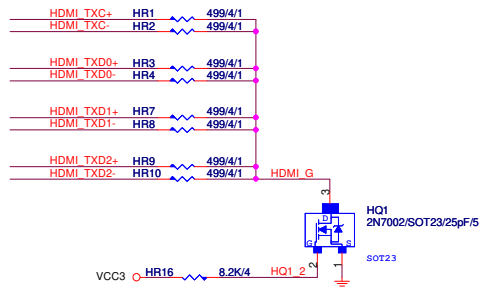
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Rev

1.01

Title

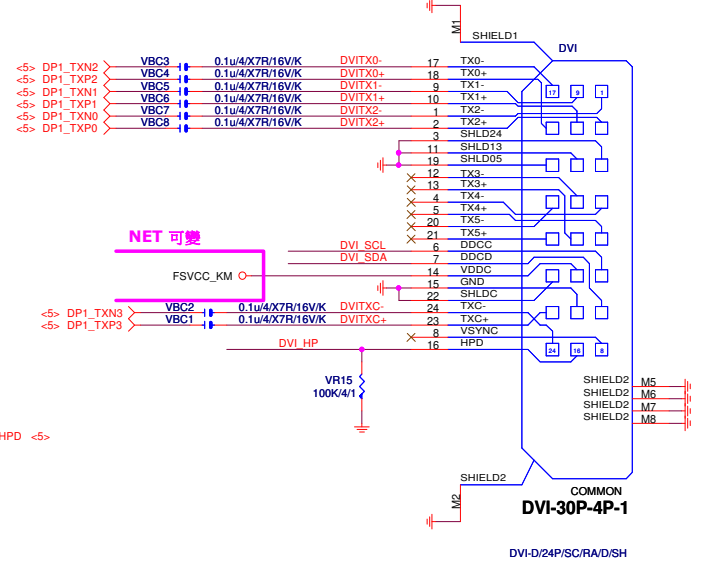
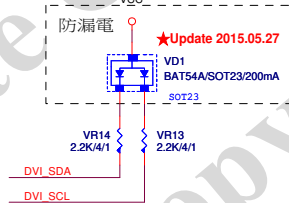
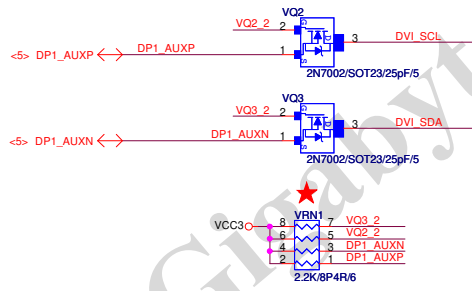
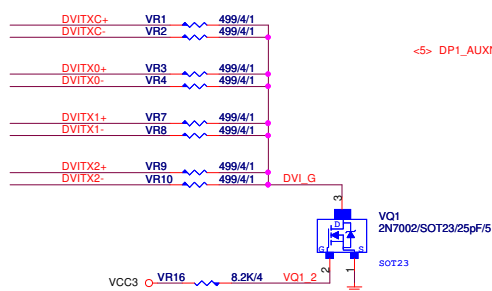
PCI EXPRESS X 16,X1



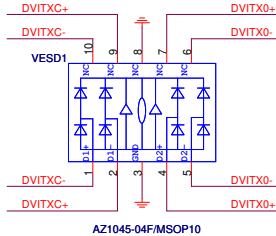
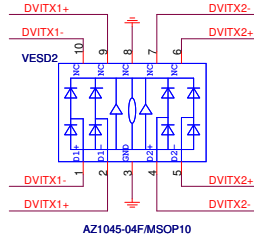
Rev: 0.73

DVI CONN

DVI :20/4/6/4/20
Impedance=85 +- 17.5%

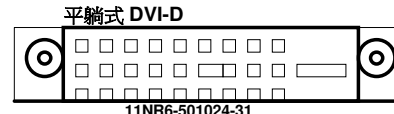


Close to connector

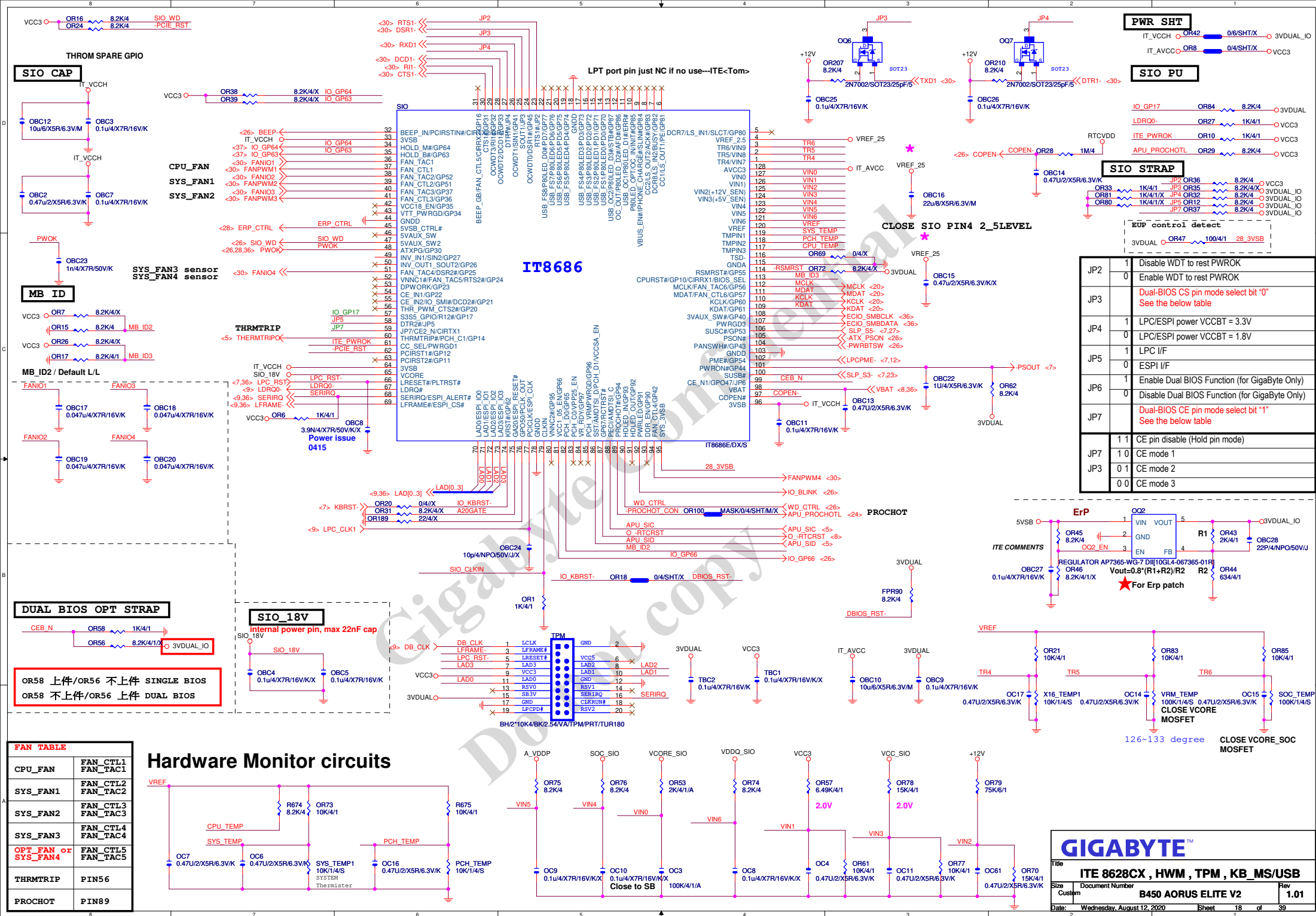


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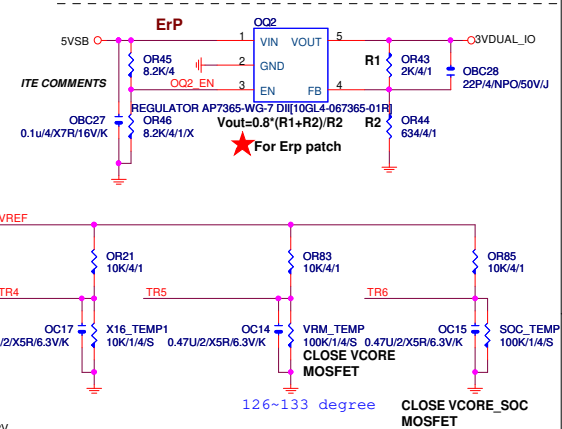
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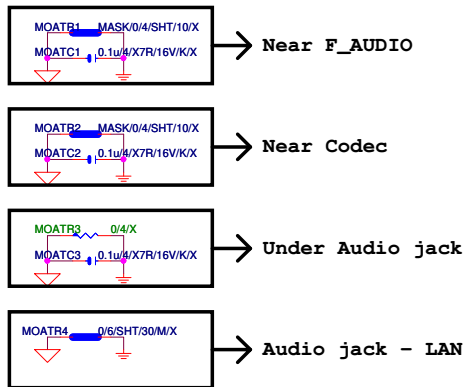


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HDMI 2.0		
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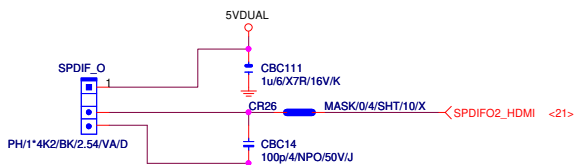


JP2	1	Disable WDT to rest PWROK
JP2	0	Enable WDT to rest PWROK
JP3		Dual-BIOS CS pin mode select bit "0" See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
JP4	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
JP5	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
JP6	0	Disable Dual BIOS Function (for GigaByte Only)
JP7		Dual-BIOS CE pin mode select bit "1" See the below table
JP7	1 1	CE pin disable (Hold pin mode)
JP7	1 0	CE mode 1
JP3	0 1	CE mode 2
JP3	0 0	CE mode 3

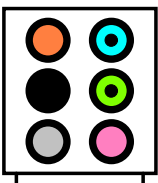




*量産前, 0ohm改short pad



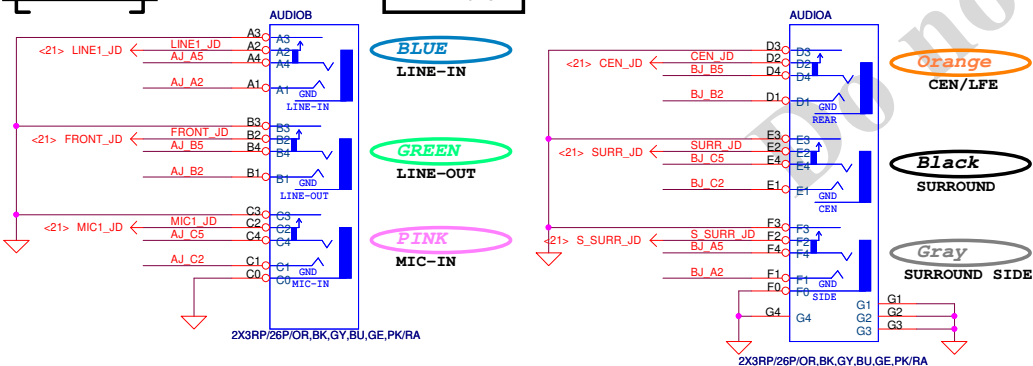
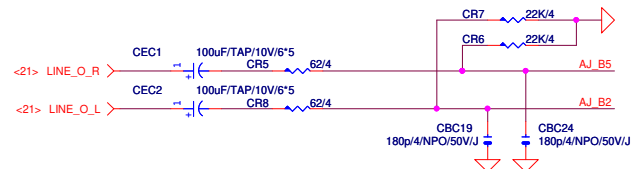
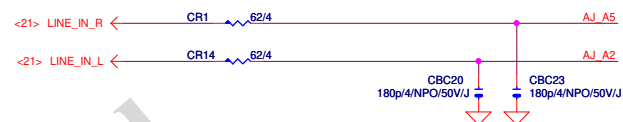
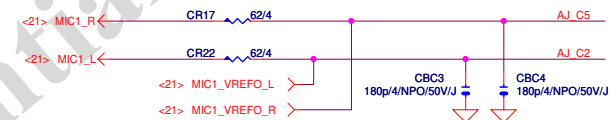
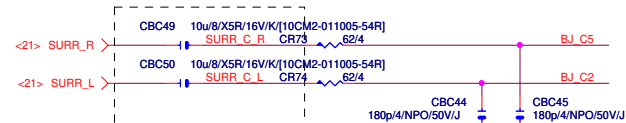
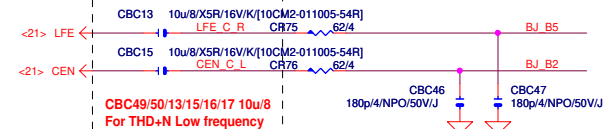
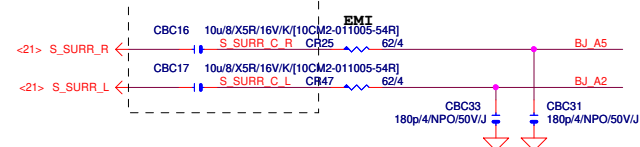
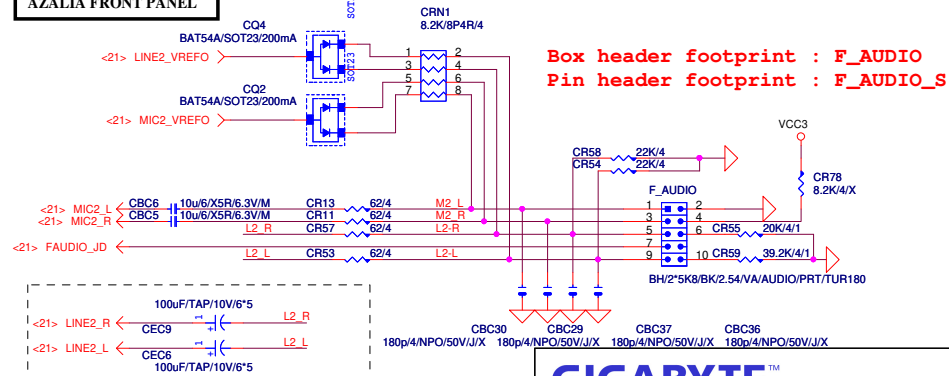
For HDMI SPDIF (依SPEC保留或移除)

AZALIA JACK**AZALIA JACK**

BLUE
LINE-IN

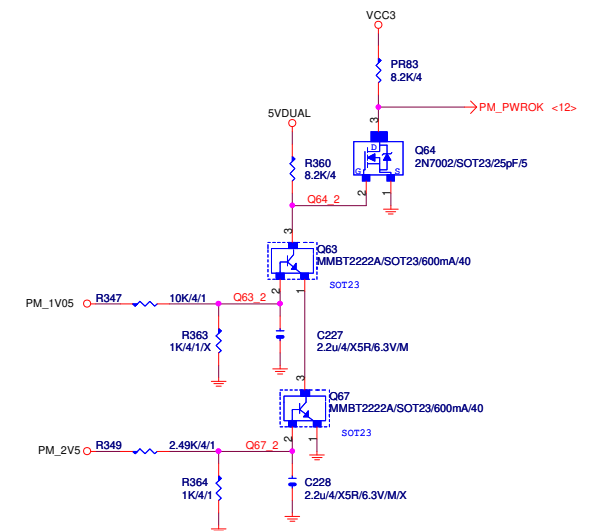
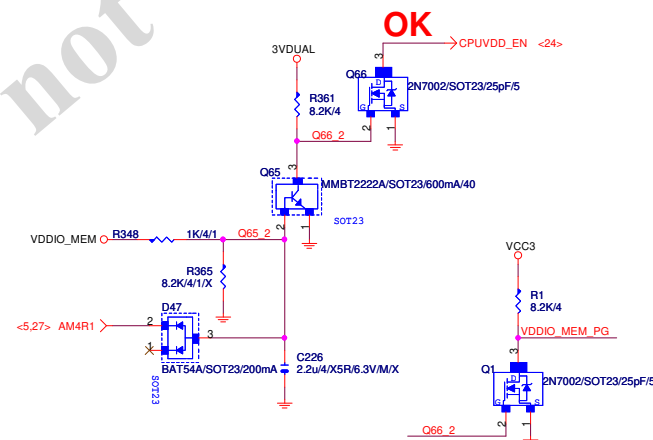
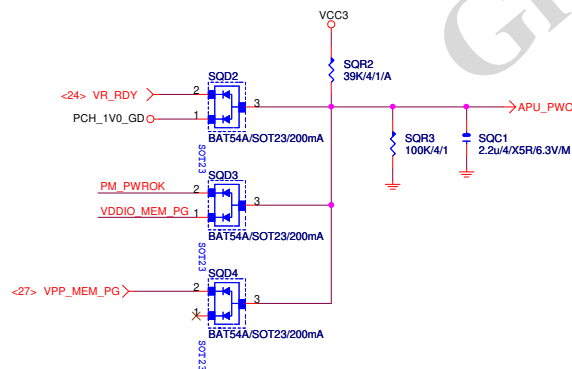
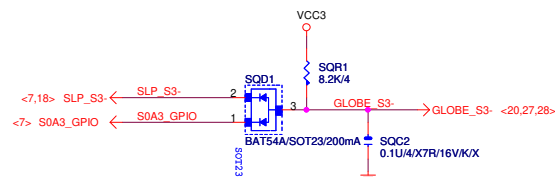
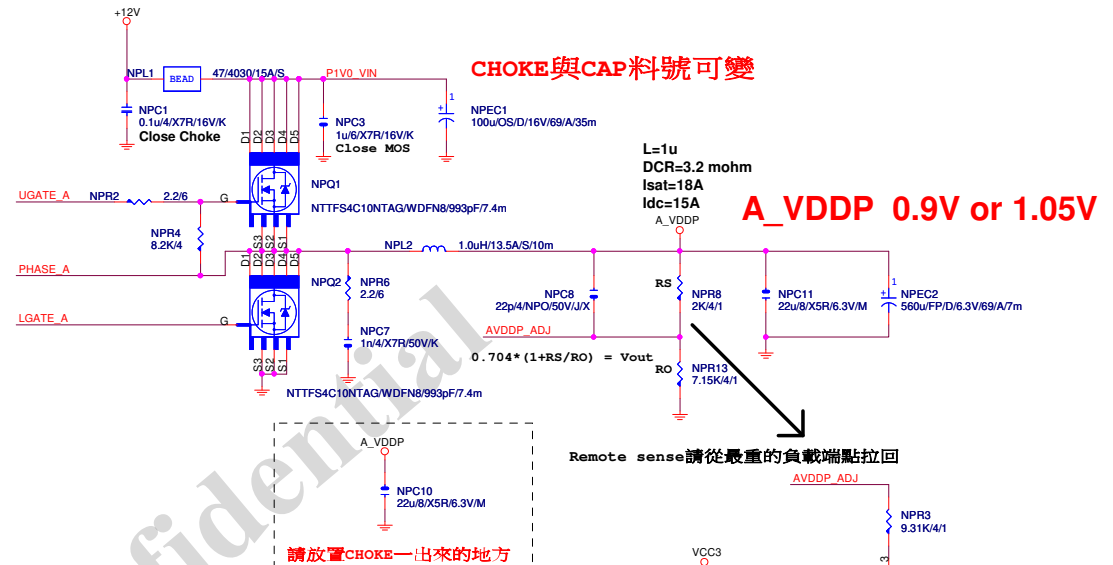
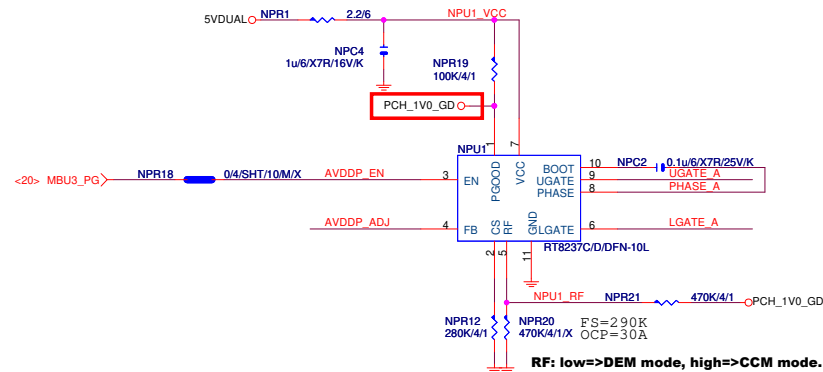
GREEN
LINE-OUT

PINK
MIC-IN

**LINE-OUT****LINE-IN****MIC-IN****SURROUND****CEN/LFE****SURR BACK****AZALIA FRONT PANEL**

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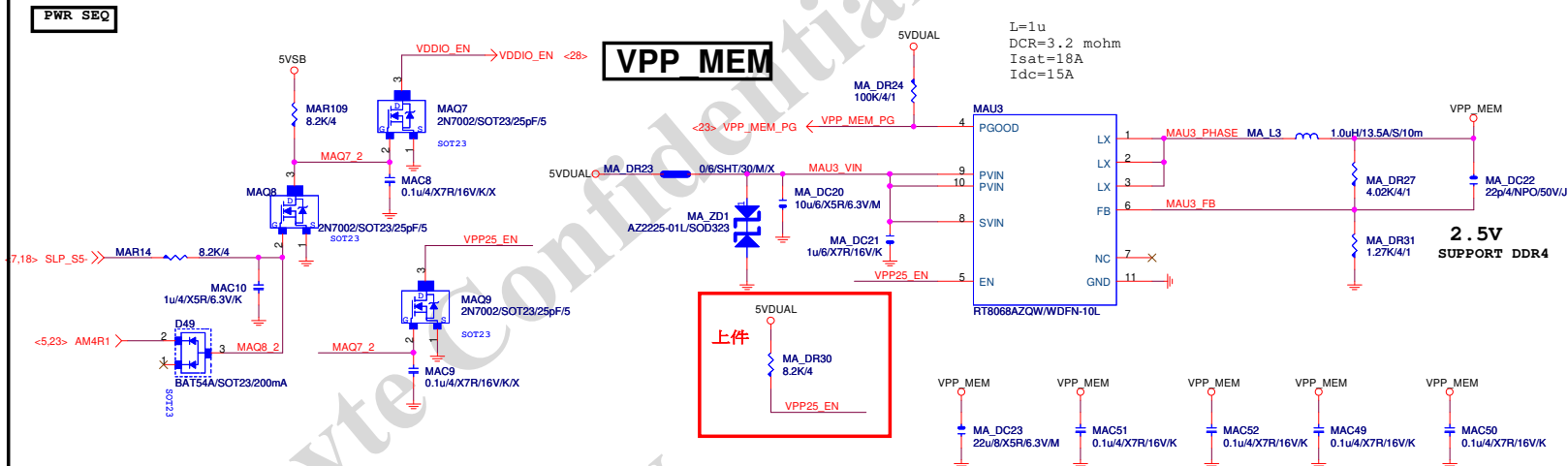
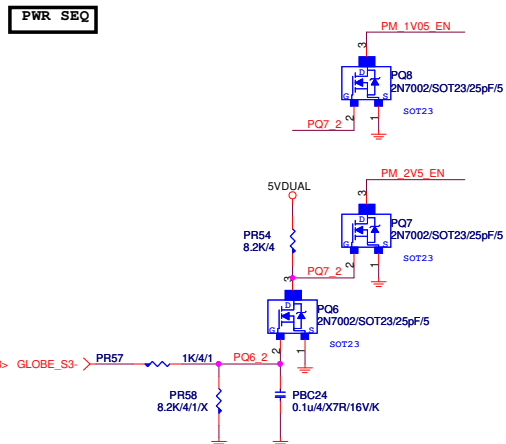
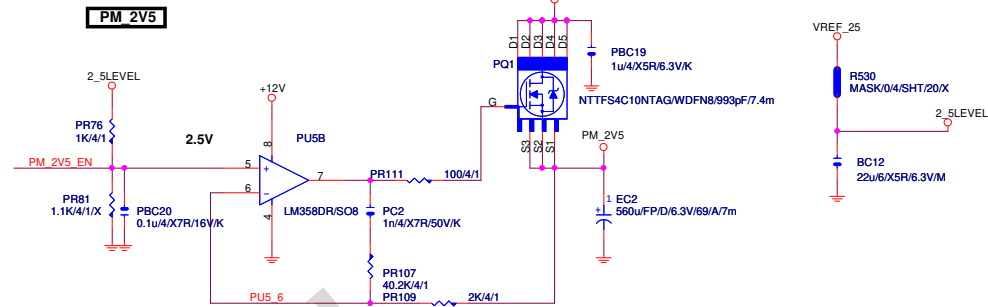
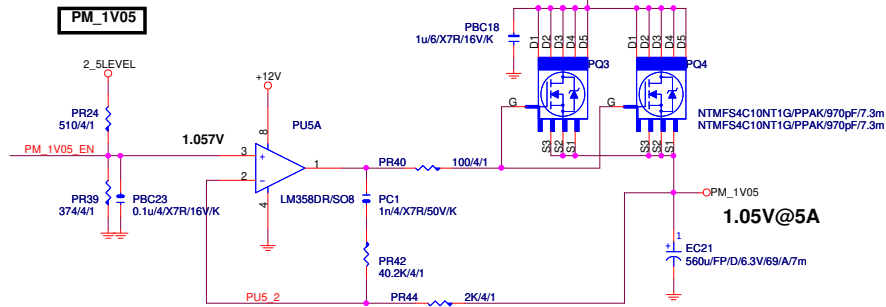
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Size			Document Number
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POWER SEQUENCE

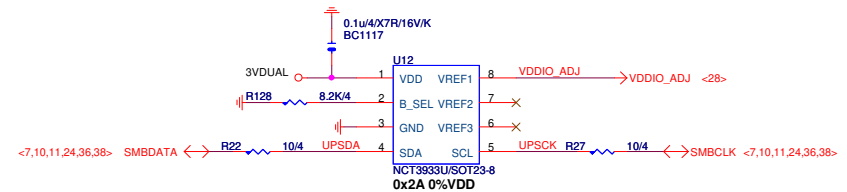
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VDDCR SOC S5

S5_MUX: S0-->High, S5-->Low
H: VDDCR_SOC_S5 will track VCORE_SOC.
L: If VCORE_SOC < 0.775V (OR 0.85V), VDDCR_SOC_S5=0.775V.
If VCORE_SOC >= 0.775V (OR 0.85V), VDDCR_SOC_S5 will trace VCORE_SOC.

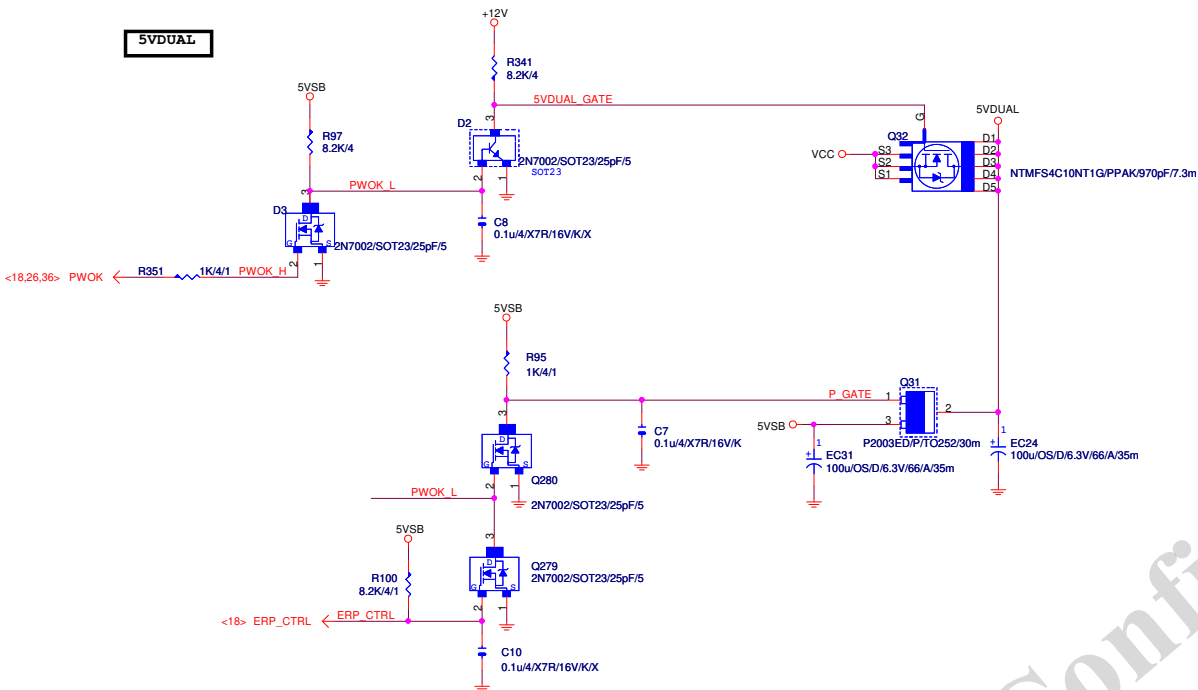
AM4 S5: 0.775V, 200mA,
S0:VAR, 900mA.



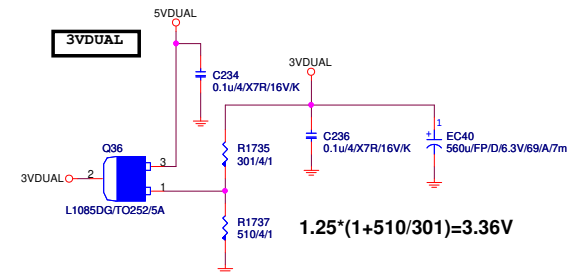
GIGABYTE

Title			
PM POWER			
Size	Document Number	Rev	
Custom	B450 AORUS ELITE V2	1.01	
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5VDUAL

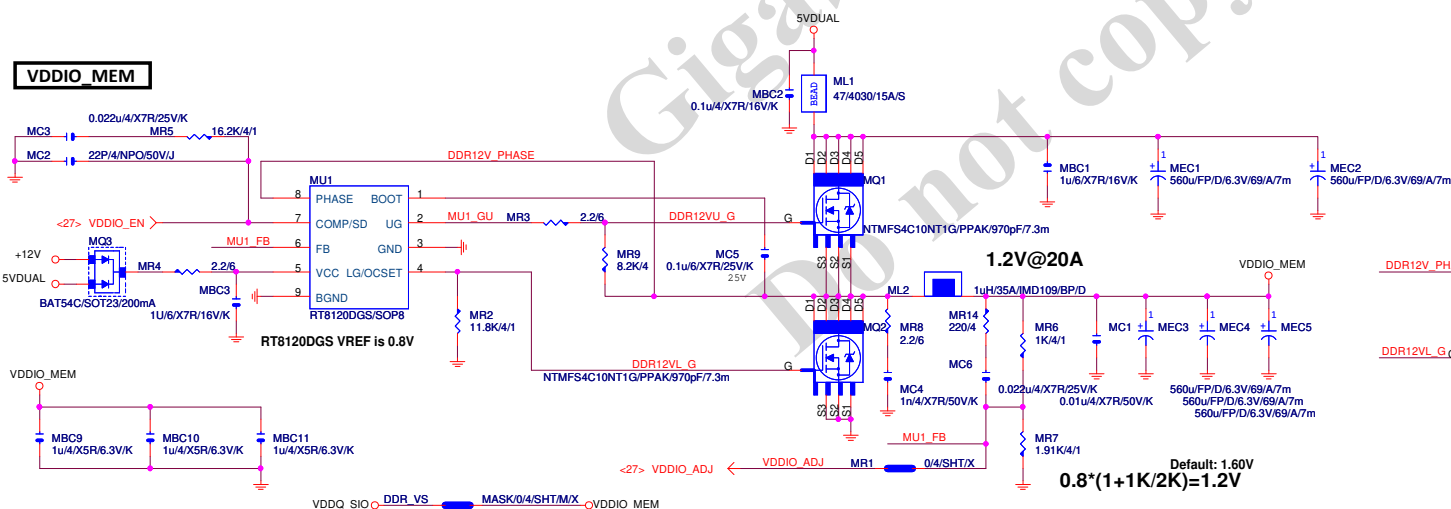


3VDUAL

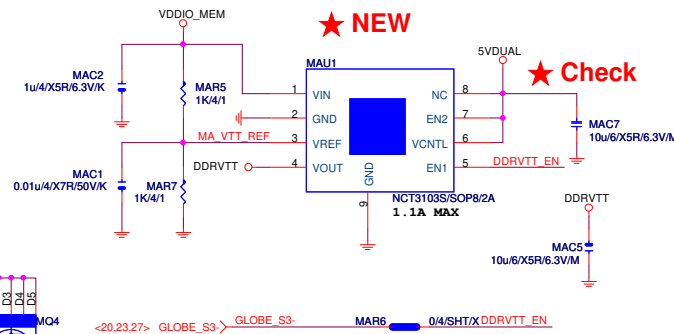


$$1.25 \times (1 + 510/301) = 3.36V$$

VDDIO_MEM

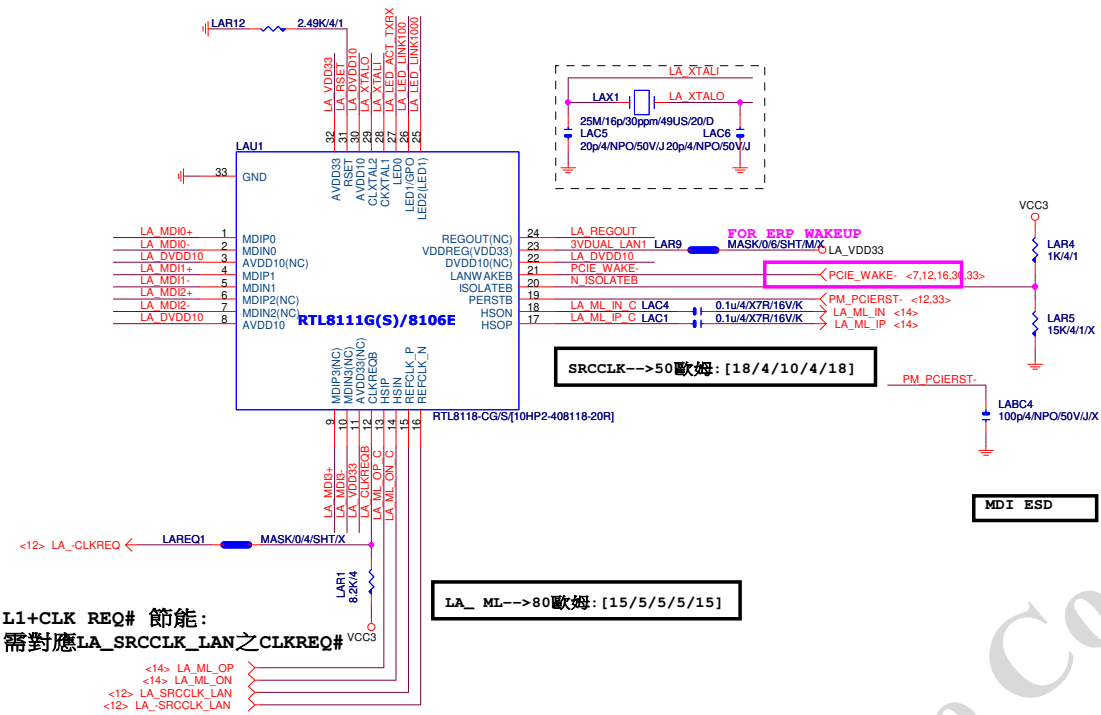


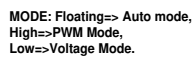
DDRVTT



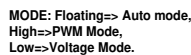
GIGABYTE

Title		
DDR PWR, 5VDUAL, 3VDUAL		
Size	Document Number	Rev
Custom	B450 AORUS ELITE V2	1.01
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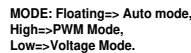




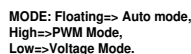
SYSTEM FAN1



SYSTEM FAN2



SYSTEM FAN3



COM PORT



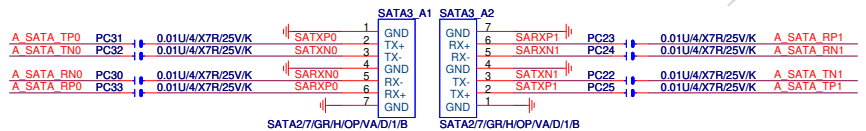
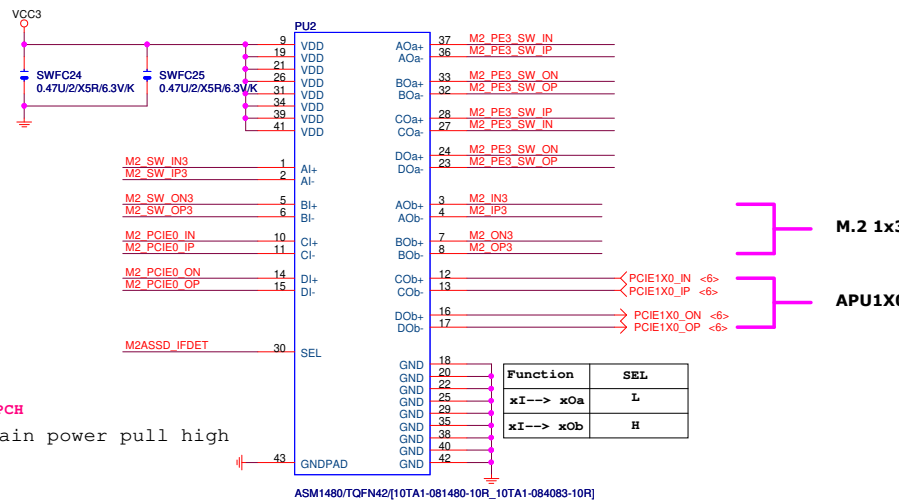
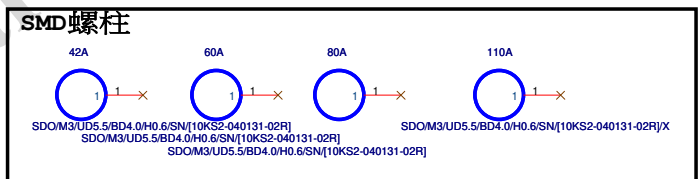
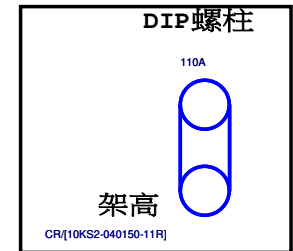
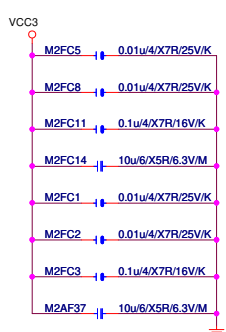
COMA

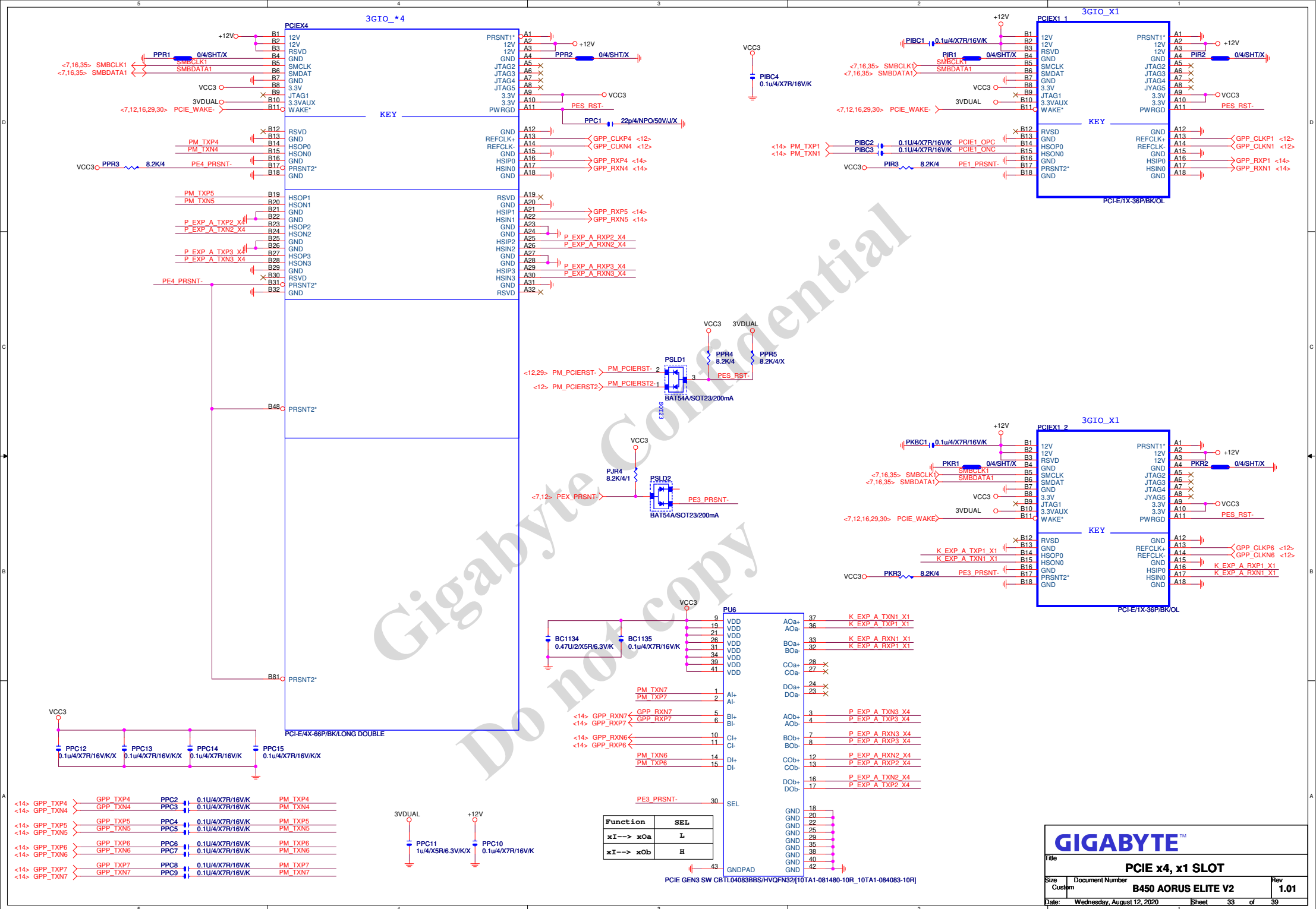


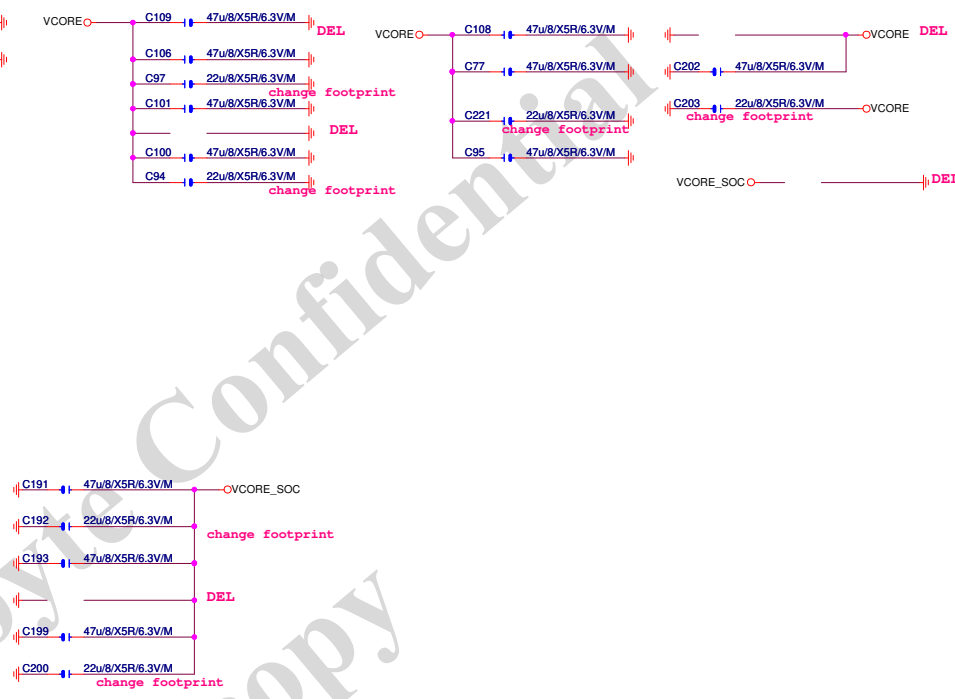
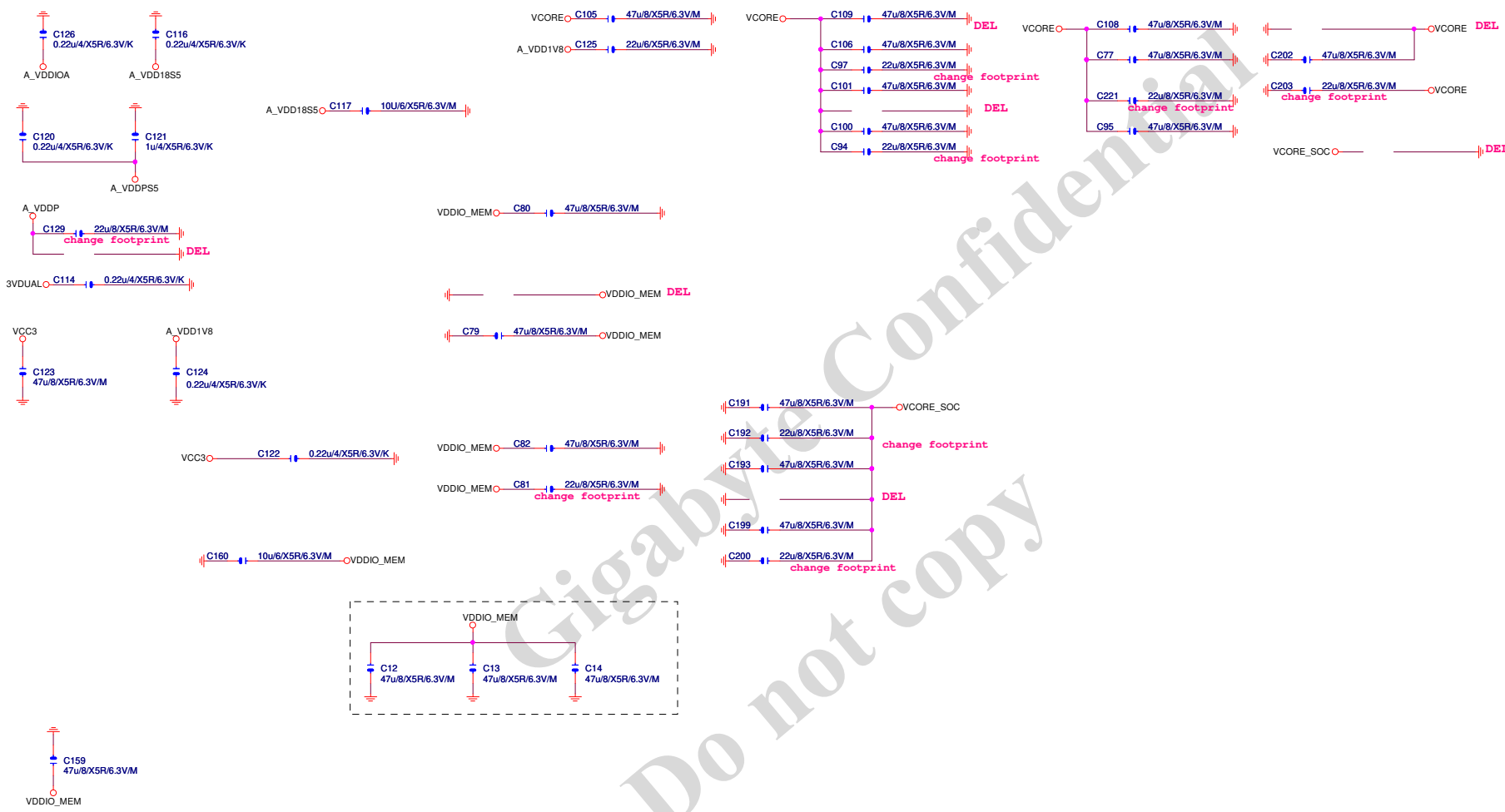
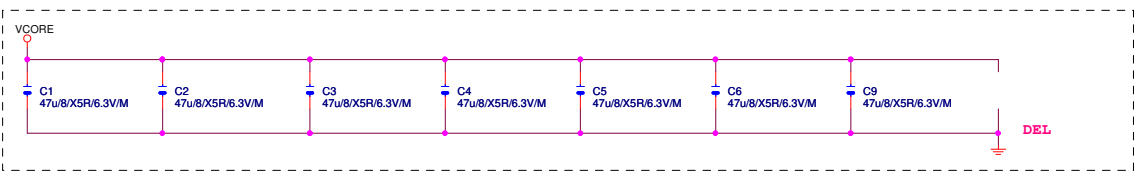
Gigabyte Confidential
Do not copy

GIGABYTETM

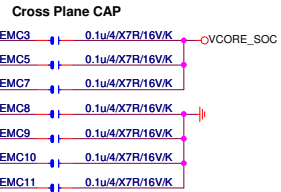
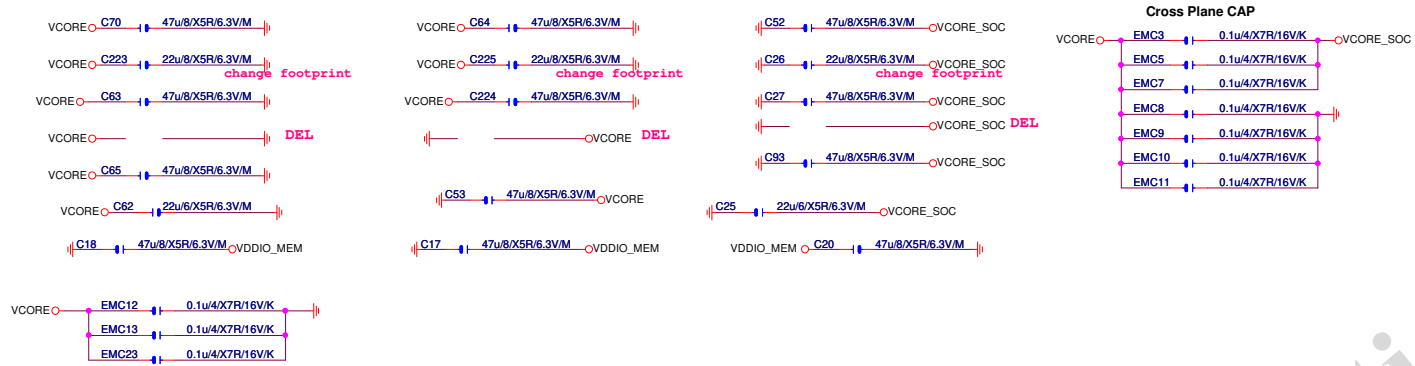
Title			DP to VGA		
Size	Document Number				Rev
Custom	B450 AORUS ELITE V2				1.01
Date:	Wednesday, August 12, 2020		Sheet	31	of 39



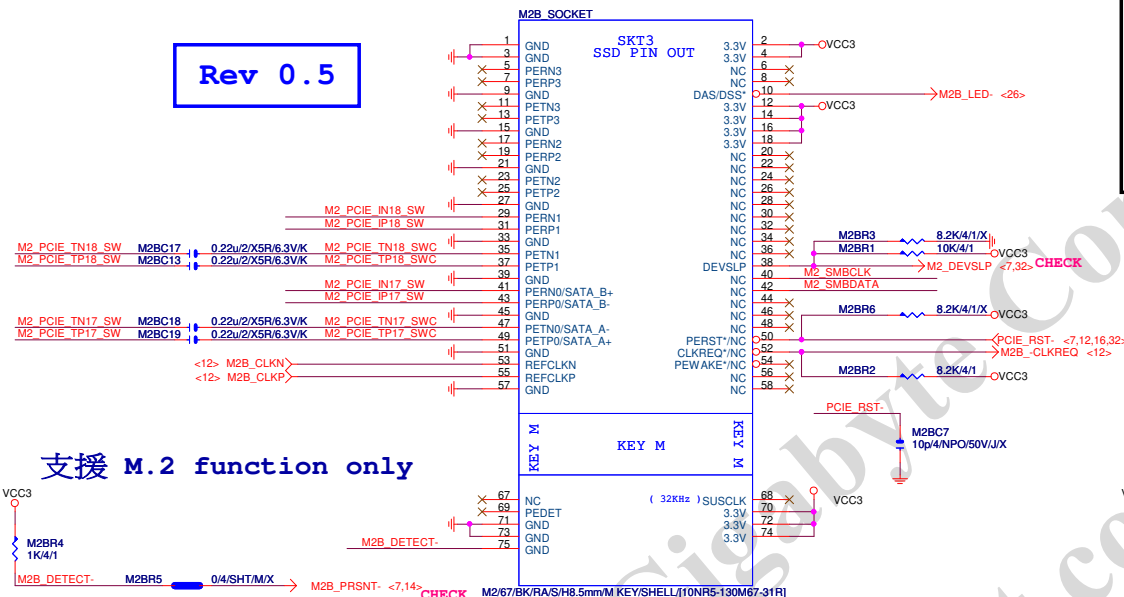




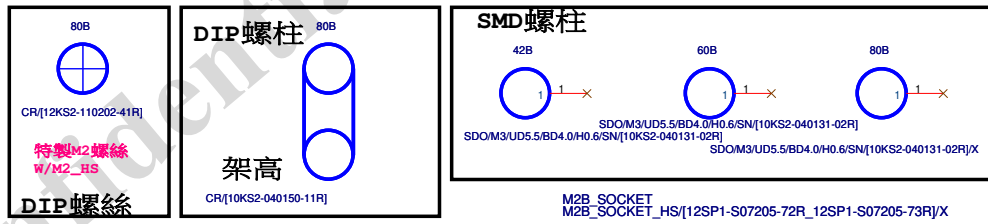
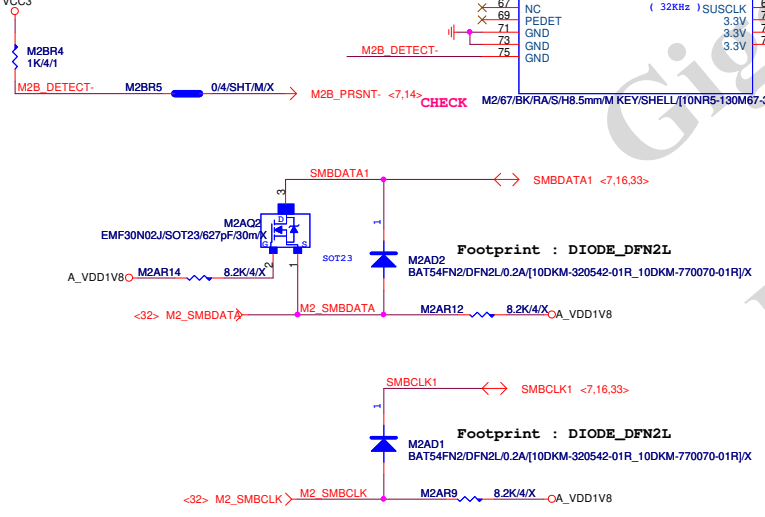
CPU TOP CAVITY



Rev 0.5



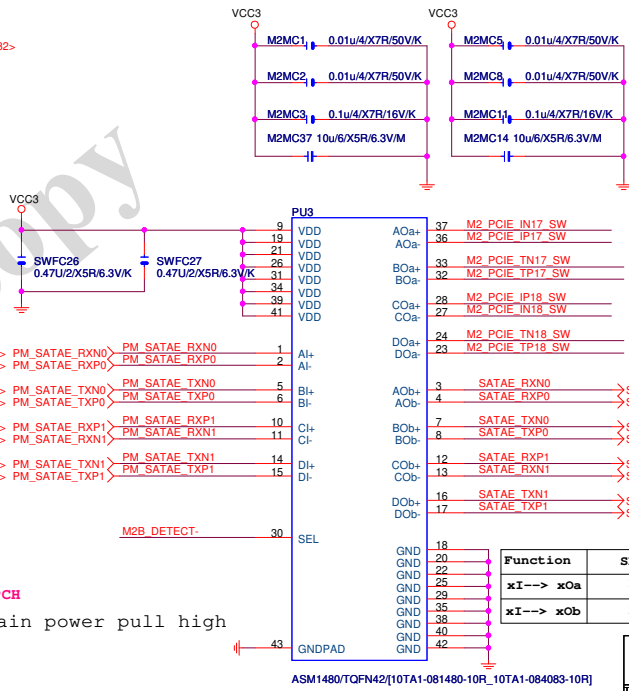
支援 M.2 function only



M2 HEATSINK

From PM SATAE

CONNECT TO PCH
BIOS設為main power pull high



To M.2B PCIE Mode

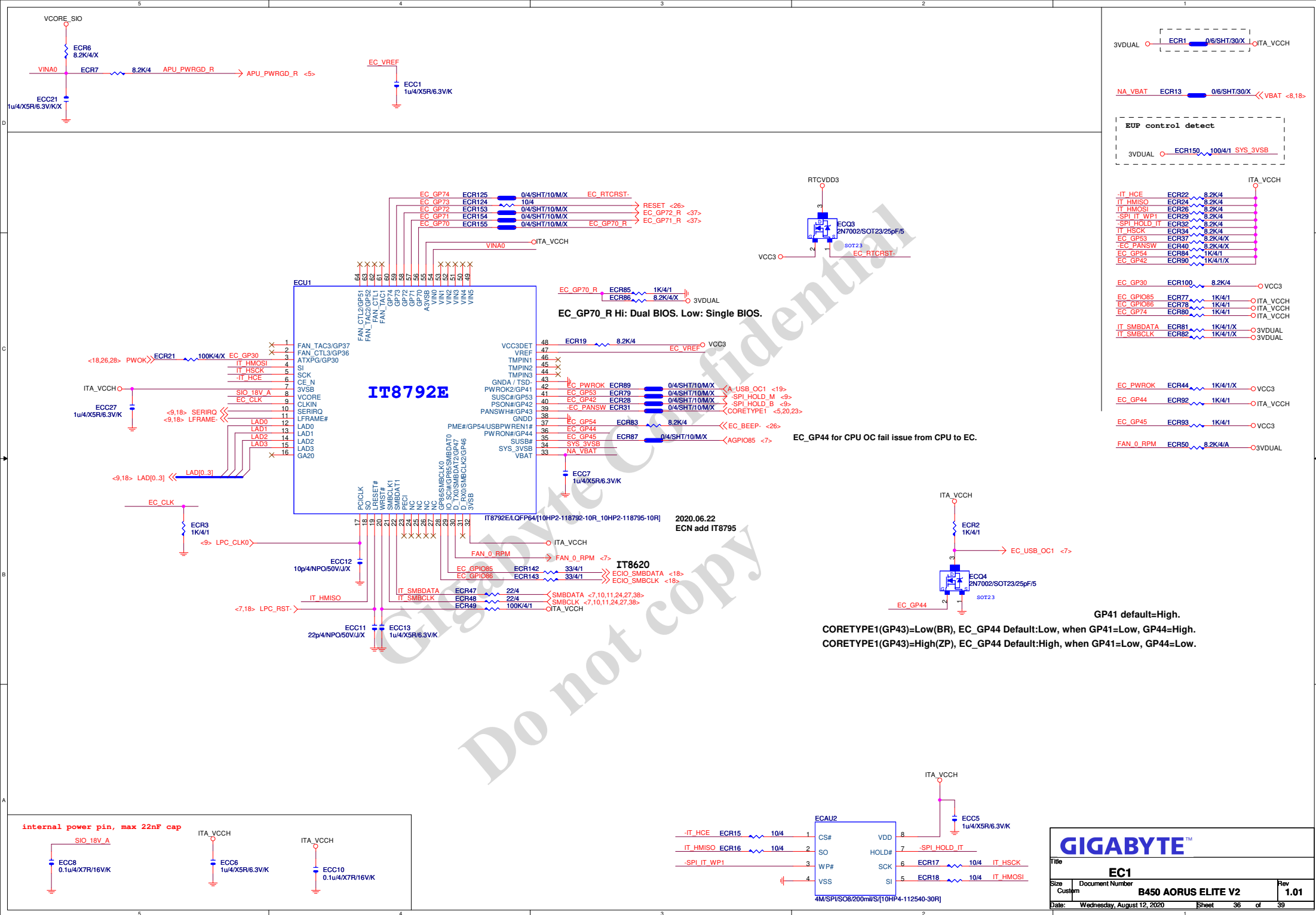
To SATA CONN

GIGABYTE

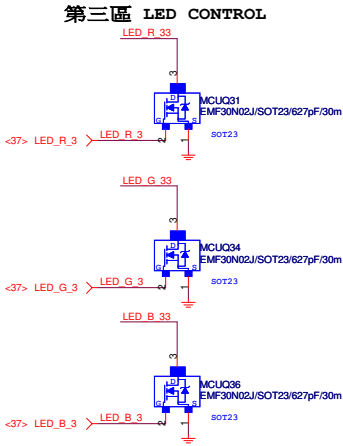
Title: **HDMI**

Size: Custom Document Number: **B450 AORUS ELITE V2** Rev: **1.01**

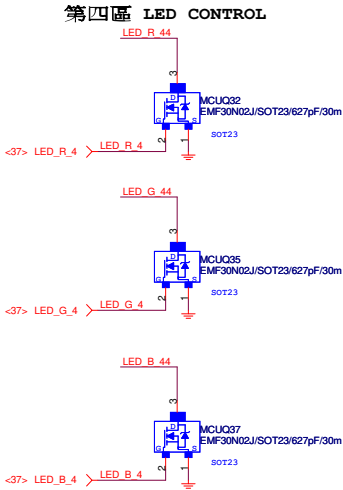
Date: Wednesday, August 12, 2020 Sheet: 35 of 39



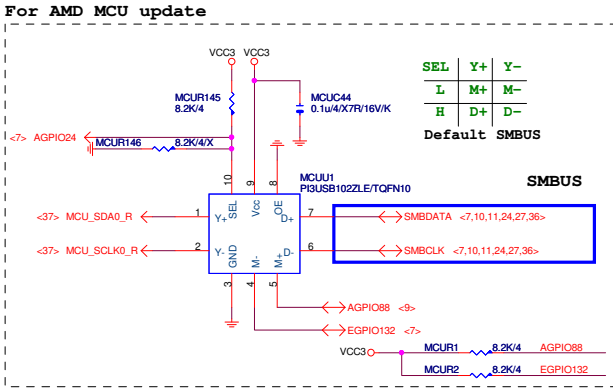
FOR PCH 正發光 LED*6 (位置在正板, 依據PCH_HS設計擺放)



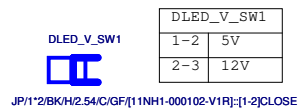
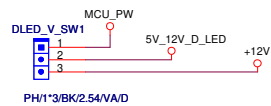
FOR AUDIO 正發光 LED*10 C_3LED1~10)



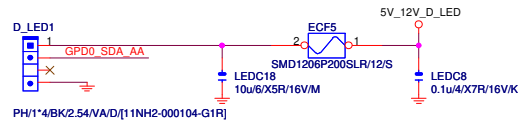
1. Debug LED (各LED依CPU/DRAM/VGA/BOOT個別位置擺放)
2. 背板 RGB LED 方向整板請統一如下
(整板正極可統一朝下或朝上)
3. 正板 RGB LED 統一方向即可
4. MCU_PW & MCU_PW33電源一律走20mils
5. ECF1,ECF2,ECF3,ECF5 兩端電源走80mils或用鋪銅方式加粗
6. MCU LED 出pin的走線4mils,如:LED_R_1,LED_G_1,LED_B_1
7. LED RGBW rule :W/S=10/5 mils 如:LED_R_11,LED_G_11,LED_B_11,LED_W.....
(包含從晶體到排阻到LED的net)
8. Digital LED NET rule W/S=4/8 mils
GPD0_SDA_B,GPD0_SDA_BB,GPD0_SDA_C,GPD0_SDA_CC



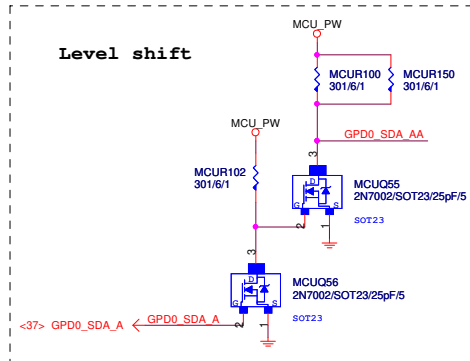
第六區 LED (靠近左上板邊位置)



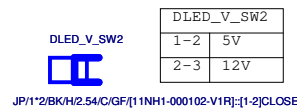
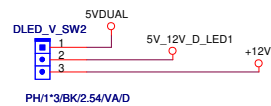
Digital LED Strip1



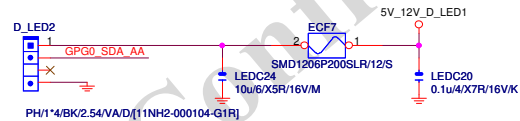
Footprint "PH1X4-CUT3-LED-L"



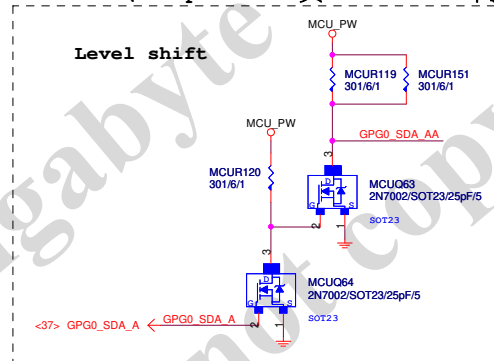
第七區 LED (靠近右下DDR板邊位置)



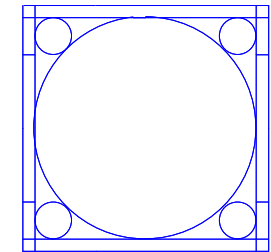
Digital LED Strip2



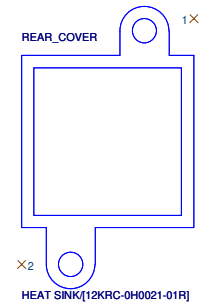
Footprint "PH1X4-CUT3-LED-L"
(for pin-name 與 model-name 同方向)



AIO_SHIELD



IO SH/SUS 430t±0.2mm AJOHO/[11AIO-0C0013-12R]



HEAT SINK[12KRC-0H0021-01R]